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10EC46

Fourth Semester B.E. Degree Examination, June/July 2018
Linear IC's and Applications

Time: 3 hrs. Max. Marks:100

Note: 1. ***Answer any FIVE full questions, selecting at least TWO questions from each part.***
2. ***Use of standard resistance (10% tolerance) and capacitance values.***

PART – A

1 a. With circuit diagram, explain the working of basic circuit of operational amplifier. **(07 Marks)**

b. A direct coupled noninverting amplifier is to amplify a 100 mV signal to a level of 3 V. Using IC741, design a suitable circuit. Assume $I_{B(max)} = 500$ nA. **(07 Marks)**

c. Write the circuit diagram of 3 input non inverting summing circuit and prove that $V_0 = V_1 + V_2 + V_3$. **(06 Marks)**

2 a. Explain the design steps to build a high input impedance capacitor coupled non-inverting voltage follower. **(06 Marks)**

b. Design a capacitor coupled inverting amplifier using IC741 to have a voltage gain of 85, output voltage amplitude of 3 V and signal frequency range from 30 Hz to 14 kHz. Assume load resistance is 1 kΩ and $I_{B(max)} = 500$ nA. **(07 Marks)**

c. Design a capacitor coupled non-inverting a amplifier using single polarity power supply is to have a 22 V supply, voltage gain of 95 V, lower cutoff frequency of 150 Hz, minimum load resistance of 7 kΩ and $I_{B(max)} = 520$ nA and output amplitude of 4.5 V. **(07 Marks)**

3 a. How upper cutoff frequency of IC741 is determined? **(07 Marks)**

b. For a voltage follower circuit using a 741 opamp, calculate the following. Assume slew rate = 0.5 V/μsec.

(i) Slew rate limited cutoff frequency if the peak of the sine wave output is 5 V.

(ii) Maximum value of the sinusoidal output voltage that will allow the circuit to operate at the 800 kHz unity-gain cutoff frequency.

(iii) Cutoff frequency limited rise time at 800 kHz unity gain cut off frequency and slew rate limited rise time if the output amplitude is 5V. **(06 Marks)**

c. Design an inverting amplifier to have a gain of 100. Input signal amplitude is 50 mV. Calculate the capacitance and resistance values to be added using Zin mod compensation method to reduce the gain to 60 dB. Assume $I_{B(max)} = 200$ nA, new cutoff frequency = 2 MHz. **(07 Marks)**

4 a. Design an instrumentation amplifier to have an overall gain of 800. The input signal amplitude is 25 mV and the supply is ±15 V. Assume $I_{B(max)} = 500$ nA and opamp 741 is used. **(10 Marks)**

b. Write the circuit diagram of precision full wave rectifier and obtain the expression for the output voltage during the positive and negative half cycle of the input. **(10 Marks)**

PART – B

5 a. Explain voltage follower peak detector. **(06 Marks)**

b. With circuit diagram, explain the circuit to generate triangular / rectangular waveform. **(07 Marks)**

c. Using 741 opamp with a supply of ±12V, design a phase shift oscillator to have an output frequency of 3.5 kHz. Assume $I_{B(max)} \triangleq 500$ nA. **(07 Marks)**

6 a. Using a bipolar opamp with ±18V supply, design an inverting Schmitt trigger circuit to have UTP = 1.5 V and LTP = −3V. Assume diode current = 500 μA, $V_F = 0.7$ V. **(10 Marks)**

b. Build a circuit to have one stable output stage using opamp and write the necessary equations to design the circuit. **(10 Marks)**

7 a. The designed dc voltage regulator has $V_S = V_{CC} = 12V$, $V_0 = 6.3V$, $R_1 = 270\Omega$. If the supply resistance is 25Ω, determine the line regulation, load regulation and ripple rejection for the circuit. IN 753 zener diode is used in the circuit. Assume $Z_Z = 7\ \Omega$, $I_{L(max)} = 42$ mA and 10% change in V_S is allowed. **(08 Marks)**

b. With circuit diagram, explain 3 terminal positive monolithic regulator and high voltage 723 regulator. **(12 Marks)**

8 a. Explain Astable multivibrator circuit using 555 timer, using the functional diagram (equations are not needed). **(10 Marks)**

b. Explain the block diagram of voltage controlled oscillator IC and obtain the expression for f_0. **(10 Marks)**

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